REMARKS

Reconsideration and allowance of the present application are respectfully requested. Claims 1-9 remain pending in the application. By this Amendment claim 1 is amended.

In numbered paragraph 2, page 3 of the final Office Action, the Examiner objects to claim 1-9 for informalities. While Applicants traverse the rejection, claim 1 is amended to address the Examiner's concern. Withdrawal of the rejection is respectfully requested.

In numbered paragraph 3, page 4 of the final Office Action, independent claim 1, along with various dependent claims, is rejected as being unpatentable over U.S. Patent 6,609,167 (Bastiani et al.) in view of U.S. Patent 6,718,413 (Wilson et al.). In numbered paragraph 4, page 7 of the final Office Action, dependent claim 9 is rejected as being unpatentable over the Bastiani et al. patent, in view of the Wilson et al. patent, and further in view of U.S. Patent 5,555,430 (Gephardt et al.). These rejections are respectfully traversed.

Applicants have disclosed a transceiver configured for use with a multi-tier system bus that allows for the flow of information to be managed among plural processors by connecting processors within modules on a local bus, which is then connected to the system bus by way of a gateway (e.g., paragraph [0014]). As exemplified in Fig. 2, a transmitter portion provides buffering and interleaved output of direct memory access and control actions packet types. A receiver portion provides input discrimination and individual buffering of direct memory access and interrupt control actions packets along with specialized control functions, e.g., reset, timer, broadcast, etc. (abstract).

Applicants have disclosed that two basic types of operations are supported, including DMA operations and control operations (e.g., paragraph [0093]). As exemplified in Fig. 2, packet buffers are separately maintained, such as a direct memory access (DMA) packet FIFO buffer 206 and a control action (CA) FIFO buffer 214 for transmission, and DMA packet FIFO buffer 212 and a control action packet FIFO buffer 210 for reception, even though they access a common system bus. Control action packet FIFO buffers (210 and 214) are maintained separate from the DMA packet FIFO buffers (206 and 212) (e.g., specification at paragraph [0085] and [0086]). Accordingly, control action operations can bypass a DMA packet FIFO buffer for bus access (e.g., specification at paragraph [00152]).

The foregoing features are broadly encompassed by claim 1, which recites a transceiver for use within a multi-tier system bus configuration, including, among other features, means for buffering instructions received via the system bus to provide a separate receive buffering of control actions from direct memory access (DMA) operations; and means for buffering instructions transmitted via the system bus to provide a separate transmit buffering of control actions from DMA operations; wherein access to the multi-tier system bus is arbitrated such that control actions preempt DMA operations.

The Examiner admits at page 4 of the final Office Action that the Bastiani et al. patent "does not explicitly teach wherein access to the multi-tier system bus is arbitrated such that control actions preempt DMA operations." Applicants respectfully submit that the Bastiani et al. patent also would not have taught or suggested means for buffering instructions received via the system bus to provide a separate receive buffering of control actions from direct memory access (DMA)

operations; and means for buffering instructions transmitted via the system bus to provide a separate transmit buffering of control actions from DMA operations, as recited in claim 1. Rather, as shown in Fig. 41, the Bastiani et al. patent merely discloses a data FIFO 356, an address counter 358, a transfer byte counter 360, and direction control, along with Host Controller Interface (HCI) registers 362, with no clear separation of buffers for transmit or receive purposes.

The Wilson et al. patent does not cure the deficiencies of the Bastiani et al. patent. The Wilson et al. patent relates to a host adapter coupled to one or more I/O devices arbitrating for the bus (abstract). The Wilson et al. patent discloses a plurality of devices in contention for a bus for data transfer to a host adapter (col. 4, lines 3-7). However, the Wilson et al. patent merely relates to SCSI devices contending for a bus in operation 606 to allow one SCSI device to transfer data to the host adapter in the operation 614 (col. 10, lines 57-65). The Wilson et al. patent would not have taught or suggested specifically means for buffering instructions received via the system bus to provide a separate receive buffering of control actions from direct memory access (DMA) operations; and means for buffering instructions transmitted via the system bus to provide a separate transmit buffering of control actions from DMA operations, as recited in claim 1. Further, the Wilson et al. disclosure is not specific to an arbitration involving access to a multi-tier system bus such that control actions preempt DMA operations, as recited in claim 1.

The Gephardt et al. patent does not cure the deficiencies of the Bastiani et al. patent and the Wilson et al. patent. The Gephardt et al. patent was applied for its disclosure of interrupt management in a multiprocessing system (col. 22, line 61 through col. 23, line 17). However, the Gephardt et al. patent would not have taught

or suggested specifically means for buffering instructions received via the system bus to provide a separate receive buffering of control actions from direct memory access (DMA) operations; and means for buffering instructions transmitted via the system bus to provide a separate transmit buffering of control actions from DMA operations, as recited in claim 1. Further, the Gephardt et al. disclosure is not specific to an arbitration involving access to a multi-tier system bus such that control actions preempt DMA operations, as recited in claim 1.

For the foregoing reasons, Applicant's claim 1 is allowable. The remaining claims depend from independent claim 1 and recite additional advantageous features which further distinguish over the documents relied upon by the Examiner. As such, the present application is in condition for allowance.

All objections and rejections raised in the Office Action having been addressed, it is respectfully submitted that the application is in condition for allowance and a Notice of Allowance is respectfully solicited.

Respectfully submitted,

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